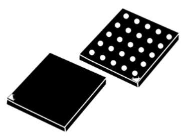
ST6G3238BE

Dual supply level translator for SD/ MINISD/ T-FLASH With ±8KV contact discharge ESD protection

Features

- High speed: t_{PD} = 4.4ns (Typ.) at T_A = 85°C V_{CCB} = 2.7V V_{CCA} = 1.8V
- Low power dissipation: I_{CCA} = I_{CCB} = 5µA (Max.) at T_A = 85°C
- Balanced propagation delays: $T_{PLH} \approx T_{PHL}$
- Power down protection on inputs and outputs
- 26Ω series resistor on A-Side
- EMI filter on B side
- Integrated pull-up and pull-down resistor on B side
- Operating voltage range:
  - V_{CCA} (Opr) = 1.4V to V_{CCB}
  - V_{CCB} (Opr) = 1.4V to 3.6V
- Latch-up performance exceeds 500mA (JESD17)
- ESD protection for card side (B port, CD and WP pins) ±8kV, IEC 61000-4-2 ESD or contact discharge:
  HBM > ±15kV (MIL STD 883 method 3015);
- ESD protection for A-port:
  HBM > ±2kV (MIL STD 883 method 3015);
- R_OHS Compliant for µTFBGA25 Package



µTFBGA25

Description

The ST6G3238BE is a dual supply low voltage CMOS Level Translator for SD/ MiniSD/ T-Flash fabricated with sub-micron silicon gate and five-layer metal wiring C^2MOS technology. Designed for use as an interface between a 3.3V bus and a 2.5V or 1.8V bus in a mixed 3.3V/1.8V, 3.3V/2.5V and 2.5V/1.8V supply systems, it achieves high speed operation while maintaining the CMOS low power dissipation. The A port is designed to track V_{CCA}. The B port is designed to track V_{CCB}.

This device is intended for two-way asynchronous communication between data buses and the direction of data transmission is determined by CMD-dir/ DATA0-dir/ DAT123-dir inputs. The B-port interfaces with the 3V bus, the A-port with the 2.5V and 1.8V bus.

All inputs are equipped with protection circuits against static discharge, giving them ±2kV (on A-side except CD and WP pins) and ±15kV on (B side, CD and WP pins) ESD immunity and transient excess voltage. See the section on integrated ESD protections and resistors for more information.

Order code

Part Number	Package	Packaging
ST6G3238BE	µTFBGA25	Tube
ST6G3238BETBR	µTFBGA25	Tape and Reel

Contents

1 Logic diagram

Figure 1. Block diagram

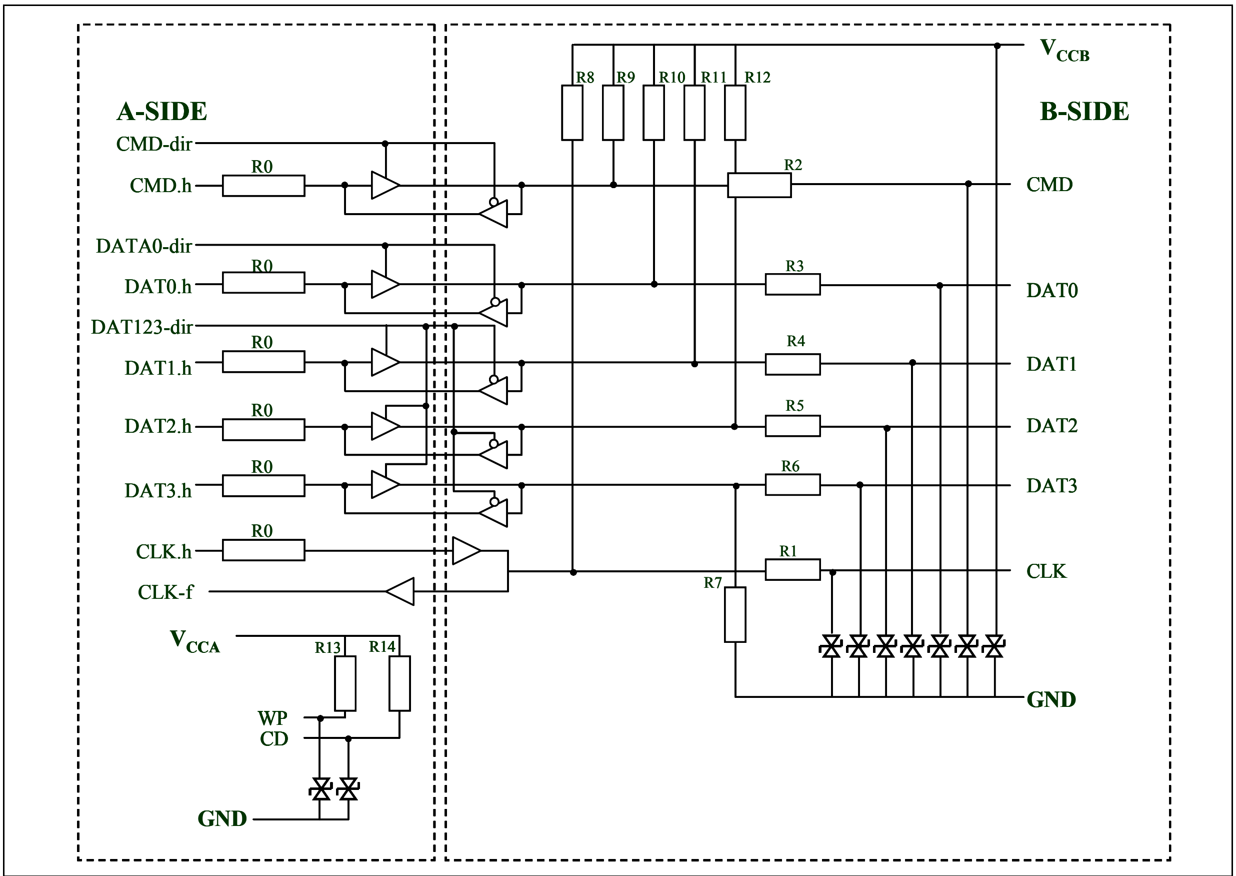


Table 1. Integrated ESD protection and resistor on B-Side

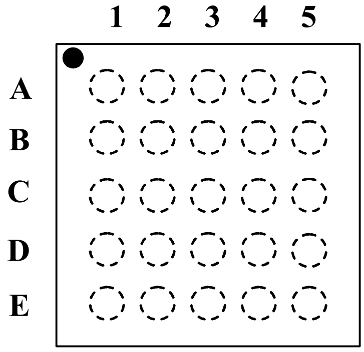
Resistors	Value	Bi-directional Zener diodes	
R1, R2, R3, R4, R5, R6	40Ω	Vbr min.	14V @ 1mA
R0	25Ω	Line capacitance	< 20 pF
Tolerance	±20%		
R10, R11, R12	70kΩ		
R9	15kΩ		
R7	470kΩ		
Tolerance	±30%		

Table 2. Integrated pull-up resistors on WP and CD pins on A-Side

Resistors	Value
R13	100kΩ
R14	100kΩ
Tolerance	±30%

2 Pin connection and function

Figure 2. Pin connection (top through view for µTFBGA)



µTFBGA25

	1	2	3	4	5
A	DAT2.h	CMD-dir	DAT0.dir	NC	DAT2
B	DAT3.h	NC	V_{CCA}	V_{CCB}	DAT3
C	CLK.h	NC	GND	GND	CLK
D	DAT0.h	CMD.h	CD	CMD	DAT0
E	DAT1.h	CLK-f	DAT123-dir	WP	DAT1

µTFBGA25

2.1 Pin function

- CMD, Command is a bi-directional line. The host and card drivers are operating in push-pull.
- DAT0-3, Data lines are bi-directional lines. The host and the card drivers are operating in push-pull mode.
- CLK, Clock is a host to card signal. CLK operates in push-pull mode.
- Feedback (return) Clock is feedback clock signal from level shifter to host for controlling delays.
- CD, Card detect, pulls HIGH state of input to V_{CCA}. This pin is protected against ESD up to 8kV contact.
- WP, Write protect, pulls HIGH state of input to V_{CCA}. This pin is protected against ESD up to 8kV contact.

Table 3. Pin description

µTFBGA Pin N°	Type	Side	Symbol	Name and function
A2	I	A-side	CMD-dir	Command direction HIGH = A to B LOW = B to A
D2	I/O	A-side	CMD.h	A-side Command
D4	I/O	B-Side	CMD	B-side Command
A3	I	A-Side	DAT0-dir	Data Direction HIGH = A to B (write) LOW = B to A (read)
D1	I/O	A-Side	DAT0.h	Data Input / Output
D5	I/O	B-Side	DAT0	Data Input / Output
E3	I	A-Side	DAT123-dir	Data Direction HIGH = A to B (write) LOW = B to A (read)
E1	I/O	A-Side	DAT1.h	Data Input / Output
A1	I/O	A-Side	DAT2.h	Data Input / Output
B1	I/O	A-Side	DAT3.h	Data Input / Output
E5	I/O	B-Side	DAT1	Data Input / Output
A5	I/O	B-Side	DAT2	Data Input / Output
B5	I/O	B-Side	DAT3	Data Input / Output
C1	I	A-Side	CLK.h	Clock Input
C5	O	B-Side	CLK	Clock Output
E2	O	A-Side	CLK-f	Clock Feedback
D3	-	A-Side	CD	Card Detect
E4	-	A-Side	WP	Write Protect
B3	-	A-Side	V_{CCA}	Power supply
B4	-	B-Side	V_{CCB}	Power supply
C3, C4	-	-	GND	Ground (0V)
A4, B2, C2	-	-	NC	No connect

3 Summary description

Table 4. Truth table

Function									Output
CMD-dir	DAT0-dir	DAT123-dir	CMD.h	CMD	DAT0.h	DAT0	DAT1.h DAT2.h DAT3.h	DAT1 DAT2 DAT3	
H	X	X	INPUT	OUTPUT	X	X	X	X	B = A
L	X	X	OUTPUT	INPUT	X	X	X	X	A = B
X	H	X	X	X	INPUT	OUTPUT	X	X	B = A
X	L	X	X	X	OUTPUT	INPUT	X	X	A = B
X	X	H	X	X	X	X	INPUT	OUTPUT	B = A
X	X	L	X	X	X	X	OUTPUT	INPUT	A = B

Note: X = Don't care; Z = High Impedance

4 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltage	-0.5 to 4.6	V
V_{CCB}	Supply voltage	-0.5 to 4.6	V
V_I	DC input voltage	-0.5 to 4.6	V
$V_{I/OA}$	DC I/O voltage (output disabled)	-0.5 to 4.6	V
$V_{I/OB}$	DC I/O voltage (output disabled)	-0.5 to 4.6	V
$V_{I/OA}$	DC output voltage	-0.5 to V_{CCA} + 0.5	V
$V_{I/OB}$	DC output voltage	-0.5 to V_{CCB} + 0.5	V
I_{IK}	DC input diode current	-20	mA
I_{OK}	DC output diode current	-50	mA
I_{OA}	DC output current	±50	mA
I_{OB}	DC output current	±50	mA
I_{CCA}	DC V_{CC} or ground current	±100	mA
I_{CCB}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation	400	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	260	°C

Table 6. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltage	1.4 to V_{CCB}	V
V_{CCB}	Supply voltage	1.4 to 3.6	V
V_I	Input voltage (CMD-dir/DAT0-dir/DAT123-dir)	0 to V_{CCA}	V
$V_{I/OA}$	I/O voltage	0 to V_{CCA}	V
$V_{I/OB}$	I/O voltage	0 to V_{CCB}	V
T_{op}	Operating temperature	-40 to +85	°C
dt/dv	Input rise and fall time (1)	0 to 10	ns/V

1. V_{IN} from 0.8V to 2.0V at V_{CC} = 3.0V

5 DC and AC parameters

Table 7. DC specification

Symbol	Parameter	Test conditions			Value				Unit
		V_{CCA} (V)	V_{CCB} (V)		T_A = 25°C		-40 to 85°C		
					Min.	Max.	Min.	Max.	
V_{IH} (A port)	High level input voltage	1.4-1.95	V_{CCA} to 3.6		0.65V_{CCA}		0.65V_{CCA}		V
		1.95-2.7			1.7		1.7		
		2.7-3.6			2.0		2.0		
V_{IL} (A port)	Low level input voltage	1.4-1.95	V_{CCA} to 3.6			0.35V_{CCA}		0.35V_{CCA}	V
		1.95-2.7				0.7		0.7	
		2.7-3.6				0.8		0.8	
V_{IH} (B port)	High level input voltage	1.4 to V_{CCB}	1.4-1.95		0.65V_{CCB}		0.65V_{CCB}		V
			1.95-2.7		1.7		1.7		
			2.7-3.6		2.0		2.0		
V_{IL} (B port)	Low level input voltage	1.4 to V_{CCB}	1.4-1.95			0.35V_{CCB}		0.35V_{CCB}	V
			1.95-2.7			0.7		0.7	
			2.7-3.6			0.8		0.8	
V_{OH} (A port)	High level output voltage	1.4-3.6	1.4-3.6	I_{OH} = -100µA	V_{CCA}-0.1		V_{CCA}-0.1		V
		1.4	1.4	I_{OH} = -1 mA	1.20		1.20		
		1.65	1.65	I_{OH} = -2 mA	1.40		1.40		
		2.3	2.3	I_{OH} = -4 mA	1.90		1.90		
		3	3	I_{OH} = -8 mA	2.45		2.45		
V_{OL} (A port)	Low level output voltage	1.4-3.6	1.4-3.6	I_{OL} = 100µA		0.10		0.10	V
		1.4	1.4	I_{OL} = 1 mA		0.20		0.20	
		1.65	1.65	I_{OL} = 2 mA		0.25		0.25	
		2.3	2.3	I_{OL} = 4 mA		0.40		0.40	
		3	3	I_{OL} = 8 mA		0.55		0.55	
V_{OH} (B port)	High level output voltage	1.4-3.6	1.4-3.6	I_{OH} = -100µA	V_{CCA}-0.2		V_{CCA}-0.2		V
		1.4	1.4	I_{OH} = -1 mA	1.05		1.05		
		1.65	1.65	I_{OH} = -4 mA	1.20		1.20		
		2.3	2.3	I_{OH} = -6 mA	1.75		1.75		
		3	3	I_{OH} = -8 mA	2.30		2.30		

Note: All A-port I/Os and control inputs are powered by V_{CCA}. All B-port I/Os are powered by V_{CCB}.

Table 7. DC specification (continued)

Symbol	Parameter	Test conditions			Value				Unit
		V_{CCA} (V)	V_{CCB} (V)		$T_A = 25°C$		-40 to 85°C		
					Min.	Max.	Min.	Max.	
V_{OL} (B port)	Low level output voltage	1.4-3.6	1.4-3.6	I_{OL} = 100µA		0.20		0.20	V
		1.4	1.4	I_{OL} = 1 mA		0.35		0.35	
		1.65	1.65	I_{OL} = 4 mA		0.45		0.45	
		2.3	2.3	I_{OL} = 6 mA		0.55		0.55	
		3	3	I_{OL} = 8 mA		0.70		0.70	
I_{IA}	Input leakage current for A-side	1.8	2.9	$V_{IA}=V_{CC}$ or GND DIR=HIGH $V_{CD}=V_{WP}=V_{CCA}$		±0.5		±5	µA
I_{IB}	Input leakage current for B-side	1.8	2.9	$V_{CLK.h}=V_{CCA}$ $V_{CMD}=V_{CCB}$ $V_{DAT0,DAT1,DAT2}=V_{CCB}$ V_{DAT3}=GND DIR=LOW $V_{CD}=V_{WP}=V_{CCA}$		±0.5		±5	µA
I_{CCA}	Quiescent supply current for A-side	1.4	1.4 - 3.6	$V_{IA}=V_{CCA}$ or GND $V_{CD} = V_{WP} = V_{CCA}$ DIR = A to B		0.5		5	µA
		1.4 - 3.6	0						
		1.4 - 3.6	3.6						
I_{CCB}	Quiescent supply current for B-side	1.4	1.4 - 3.6	$V_{CLK.h}=V_{CCA}$ or GND V_{IB}=OPEN DIR = B to A $V_{CD} = V_{WP} = V_{CCA}$		0.5		5	µA
		1.4 - 3.6	3.6						
I_{WP}	WP pin input leakage current	1.8	3.0	$V_{IA}=V_{CCA}$ or GND DIR=HIGH V_{WP}=GND		36			µA
I_{CD}	CD pin input leakage current	1.8	3.0	$V_{IA}=V_{CCA}$ or GND DIR=HIGH V_{CD}=GND		36			µA

Table 8. AC electrical characteristics (f = 1MHz, 50% duty cycle, C_L = 30pF, R_L = 500Ω)

Symbol		Parameter	Test condition T_A = -40 to 85 °C						Unit
			V_{CCA} = 1.8 ± 0.15V		V_{CCA}=1.8 ± 0.15V		V_{CCA}=2.5 ± 0.2V		
			V_{CCB}=2.5 ± 0.2V		V_{CCB}=2.7 ± 0.3V		V_{CCB}=2.7 ± 0.3V		
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}		Propagation delay time An to Bn	1.0	7.2	1.0	6.6	1.0	6.1	ns
t_{PLH} t_{PHL}		Propagation delay time Bn to An	1.0	5.8	1.0	5.4	1.0	4.8	
t_{OSLH} t_{OSHL}		Output to output skew time (1)(2)		0.5		0.5		0.5	ns
t_{CDLH} t_{CDHL}		Clock and data skew time		0.5		0.5		0.5	ns
f_{max}	Clock	From A to B	52		52		52		MHz
		From B to A	52		52		52		
	Data	From A to B	52		52		52		Mbps
		From B to A	52		52		52		

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = | t_{PLHm} - t_{PLHn} |, t_{OSHL} = | t_{PHLm} – t_{PHLn} |)
2. Parameter guaranteed by design.

Table 9. Output slew rate (f = 1MHz, 50% duty cycle, CL=30pF, RL=500Ω)

Symbol	Parameter	From	To	Test condition T_A = -40 to 85 °C		Unit
				V_{CCA} = 1.8V ± 0.15V V_{CCB} = 3V ± 0.3V		
				Min.	Max.	
t_r	Rise time	20%	80%		3	ns
t_f	Fall time	80%	20%		3	ns

Table 10. Capacitance characteristics

Symbol	Parameter	Test condition			Value					Unit
		V_{CCB} (V)	V_{CCA} (V)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
C_{INB}	Input capacitance	open	open			9				pF
$C_{I/OA}$	Input/Output capacitance for A-SIDE	3.3	2.5			17				pF
$C_{I/OB}$	Input/Output capacitance for B-SIDE	3.3	2.5			33				pF
C_{PD}(1)	Power dissipation capacitance	3.3	2.5	f = 10MHz		29				pF
		3.3	1.8			29				

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current can be obtained by the following equation. I_{CC}(opr) - C_{PD} x V_{CC} x f_{IN} + I_{CC}/16 (per circuit)

Note: V_{IA} = Input I/Os including CLK.h, CMD.h, DAT0.h, DAT1.h, DAT2.h, DAT3.h
V_{IB} = Input I/Os including CMD, DAT0, DAT1, DAT2, DAT3

6 I/O and test circuit

Figure 3. Input and output equivalent circuit

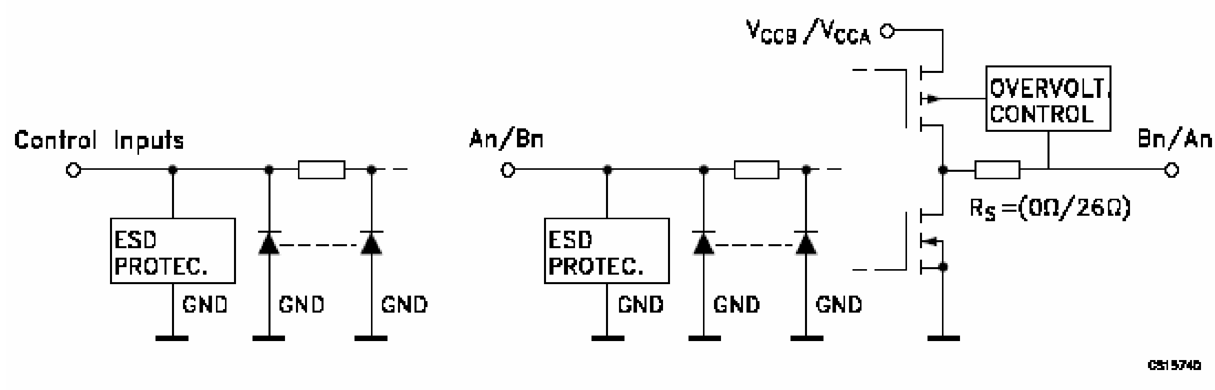


Figure 4. Test cicuit

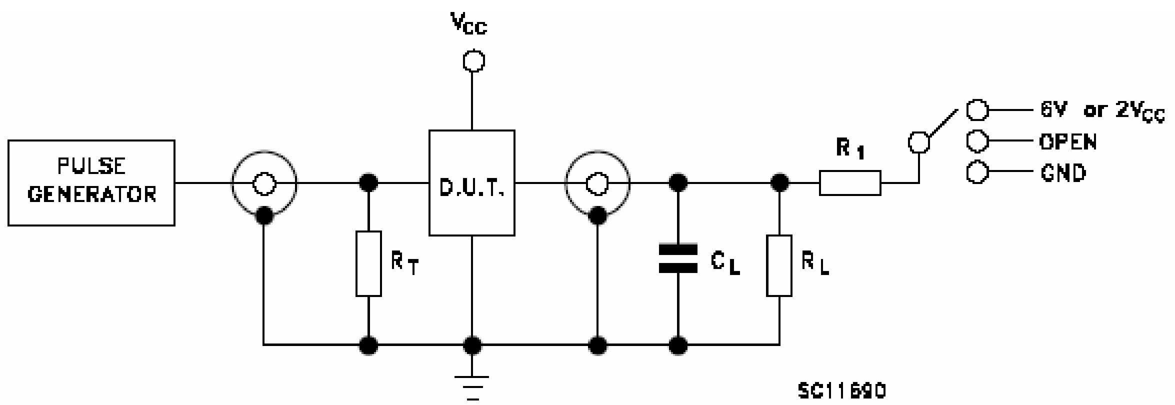


Table 11. Test values

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZ}L, t_{PLZ} (V_{CC} = 3.0 to 3.6V)	6V
t_{PZL}, t_{PLZ} (V_{CC} = 2.3 to 2.7V or V_{CC} = 1.6 to 1.95V)	$2V_{CC}$
t_{PZH}, t_{PHZ}	GND

7 Waveforms

Figure 5. Waveform - propagation delay (f = 1 MHz, 50% duty cycle)

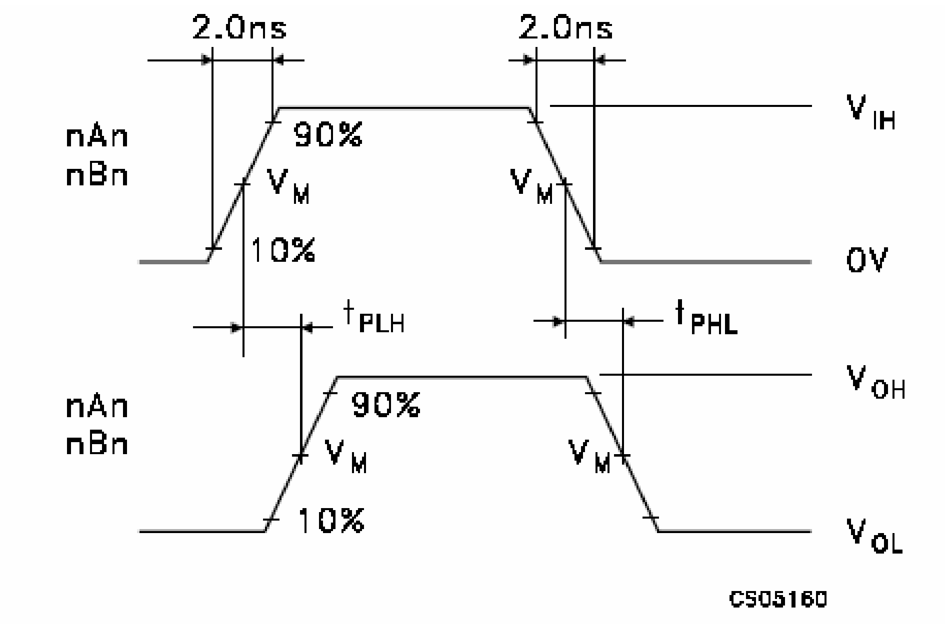


Table 12. Waveform symbol value

Symbol	V_{CC}		
	3.0 to 3.6V	**2.3 to 2.7V**	**1.65 to 1.95V**
V_{IH}	V_{CC}	V_{CC}	V_{CC}
V_M	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL}+0.3V	V_{OL}+0.15V	V_{OL}+0.15V
V_Y	V_{OL}-0.3V	V_{OL}-0.15V	V_{OL}-0.15V

Note: *C_L = 30pF or equivalent (includes jig and probe capacitance)*

R_L = R1 = 500Ω or equivalent

R_T = Z_{OUT} of pulse generator (typically 50Ω)

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 13. µTFBGA25 mechanical data

Dim Ref	Dimension (mm)			Dimension (inch)		
	Min.	Typ.	Max	Min.	Typ.	Max
A	1.0	1.10	1.16	0.039	0.043	0.046
A1			0.25			0.010
A2	0.78		0.86	0.031		0.034
b	0.25	0.30	0.35	0.010	0.012	0.014
D	2.90	3.0	3.10	0.114	0.118	0.122
D1		2.0			0.079	
E	2.90	3.0	3.10	0.114	0.118	0.122
E1		2.0			0.079	
e		0.50			0.020	
SE		0.25			0.010	

Figure 6. Package dimensions

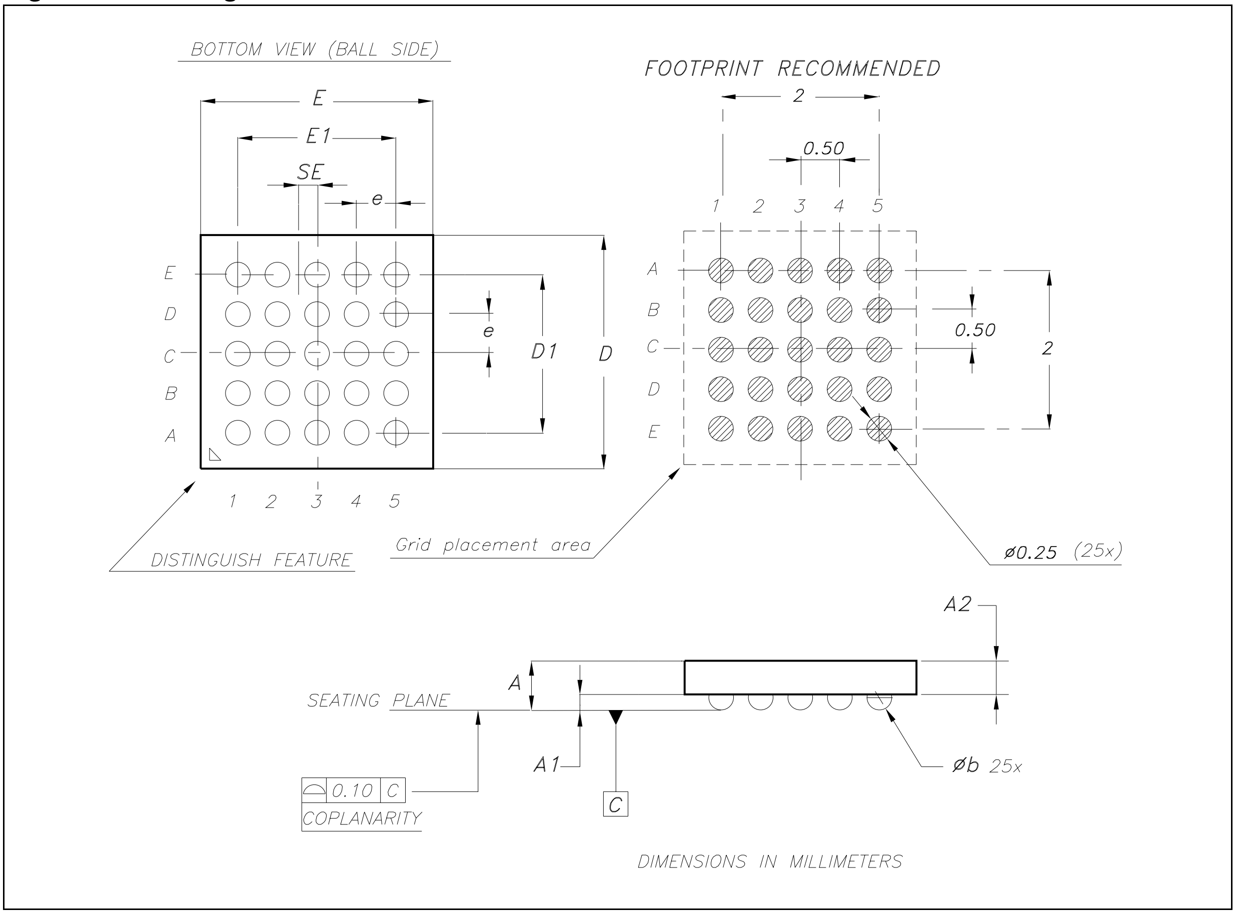
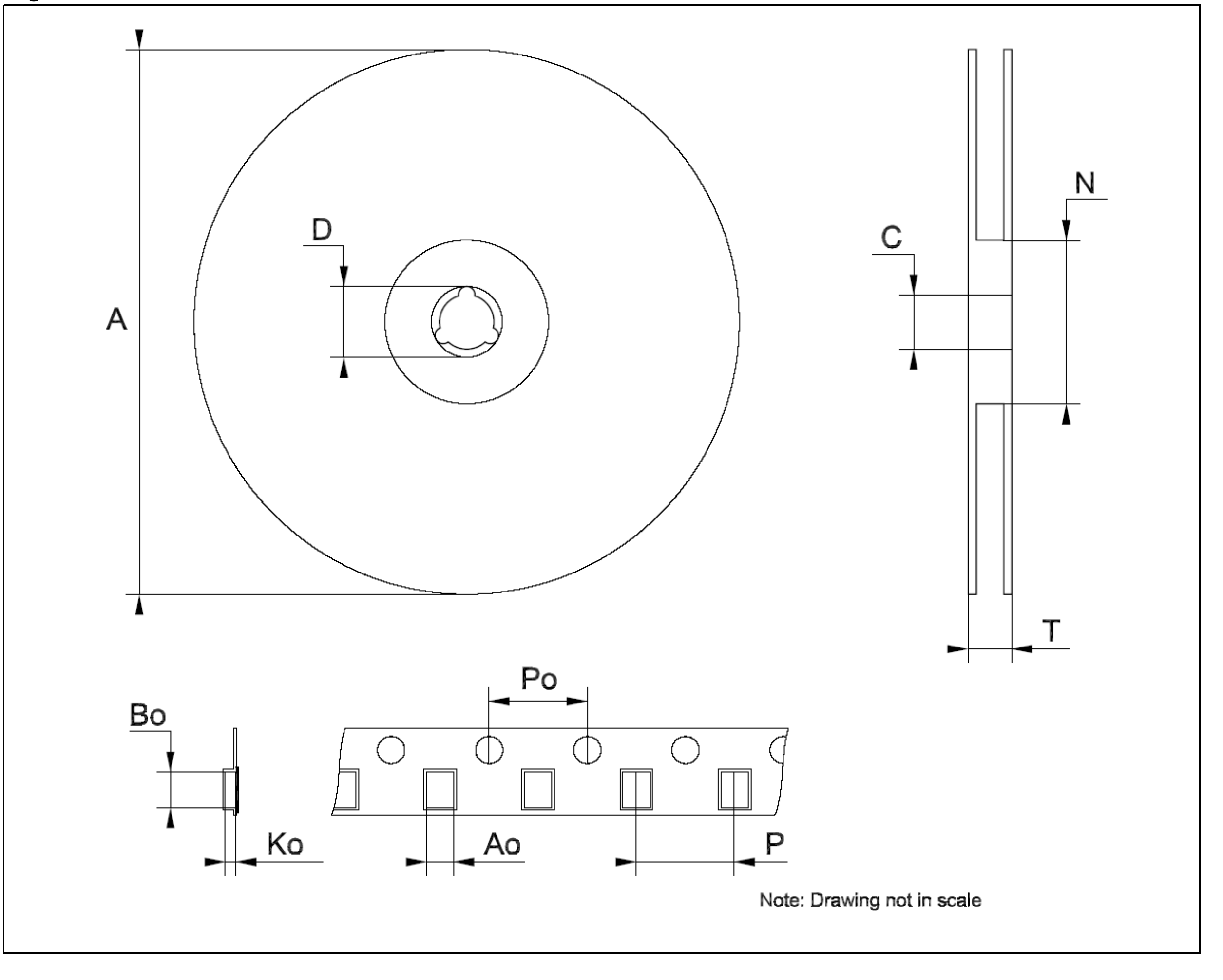


Table 14. µTFBGA25 tape and reel information

Dim Ref	Dimension (mm)			Dimension (inch)		
	Min.	Typ.	Max	Min.	Typ.	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.60			0.063	
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

Figure 7. Reel dimension



9 Revision history

Table 15. Revision history

Date	Revision	Change
22-Mar-2007	1	First release

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